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DATE MAILED: 10/03/2002

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,864	03/31/2000	Yasuaki Seki	0010-1098-0	9265
·	7590 10/03/2002			
Oblon Spivak McClelland Maier & Neustadt PC 1755 Jefferson Davis Highway Fourth Floor			EXAMINER	
Arlington, VA		PATEL, ISHWARBHAI B		VARBHAI B
			ART UNIT	PAPER NUMBER
			2827	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
·	09/539,864	SEKI ET AL.				
Office Action Summary	Examiner	Art Unit				
	Ishwar (l. B.) Patel	2827				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status						
1) Responsive to communication(s) filed on <u>09 S</u>	September 2002 .					
	s action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims						
4)⊠ Claim(s) <u>11-26</u> is/are pending in the application.						
4a) Of the above claim(s) 11-18 is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>19-26</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers	,					
9)☐ The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>07 May 2002</u> is/are: a)□ accepted or b)⊠ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
11)☐ The proposed drawing correction filed on is: a)☐ approved b)☐ disapproved by the Examiner.						
If approved, corrected drawings are required in reply to this Office action.						
12)☐ The oath or declaration is objected to by the Examiner.						
Priority under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)⊠ All b)□ Some * c)□ None of:						
 Certified copies of the priority documents 	have been received.					
2. Certified copies of the priority documents have been received in Application No						
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).						
a) The translation of the foreign language provisional application has been received.						
15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121. Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4) Interview Summary (PTO-413) Paper No(s) 5) Notice of Informal Patent Application (PTO-152) 6) Other:						

Application/Control Number: 09/539,864 Page 2

Art Unit: 2827

DETAILED ACTION

Election/Restrictions

1. Restriction requirement is maintained. Claims 11-18, directed to a method for producing a multilayer printed wiring board comprising plasma etching a layer of an insulating resin composition and forming a conductive layer on the said insulating layer, remain withdrawn from consideration as being directed to a non-elected invention. The method for producing multiplayer printed wiring board is classified in class 29, subclass 846. Further, the method can be used for producing a different product, such as for producing a conductive laminate instead of a printed circuit board, or for producing a single layer circuit board instead of a multiplayer circuit board. Even the plasma etching alone can be used for cleaning the drilled via hole or for cleaning the surface of insulating or conductive layer.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

2. The drawings are objected to because figures are improperly crosshatched. All of the parts shown, and only those parts, must be crosshatched. The cross hatching pattern should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Art Unit: 2827

Claim Rejections - 35 USC § 112

- 3. The following is a quotation of the second paragraph of 35 U.S.C. 112:
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 4. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear what is meant by "the first resin and the second resin are not compatible with each other". The term "compatible" is very general and vague. It is not clear what kind of compatibility / non compatibility is claimed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily

Art Unit: 2827

published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 19 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Shinada et al., US Patent 6,121,553, hereafter Shinada.

Shinada discloses a multiplayer printed wiring board comprising: an insulating resin layer and a conductive layer (various examples of circuit boards described including examples 18, 21 with adhesive layer 12, column 23 and column 26),

wherein said resin composition comprises a first resin and a second resin and said first and said second resin have different plasma etching rates (adhesive layers made form a thermosetting adhesive layers made from a thermosetting adhesive composition comprising a polyamide-imide resin and a thermosetting component, and the polyamide-imide resin and epoxy resin have different dry etching rate). Though, Shinada does not disclose the plasma etching of the insulating resin layer, the circuit board of Shinada has inherent structure of a multiplayer circuit board. Further, the plasma etching is process limitation in the product claim. Such a process limitation defines the claimed invention over the prior art to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as or obvious over the prior art. See product-by-process in MPEP 2113 and 2173.05(p) and In *re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claim 24, Shinada further discloses the insulation layer formed on a surface of a substrate and said substrate comprises a wiring pattern on said surface of said substrate, see figure 3A-3D and 5A-5D.

Regarding claim 25, Shinada further discloses holes in said insulating layer to expose a portion of said wiring pattern, see figure 3A-3D and 5A-5D.

Claim Rejections - 35 USC § 103

7. Claims 20-23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinada et al., US Patent 6,121,553 as applied to claim 19 above, and further in view of Burke et al. US Patent 6,042,929, hereafter Burke, Enomoto et al., US Patent 5,055,321, hereafter Enomoto and Yasumoto et al., US Patent No. 6,040,068, hereafter referred to as Yasumoto.

Regarding claim 20, the applicant is claiming the plasma treated insulation layer has surface roughness of 100 nm to 4000 nm. Though, Shinada does not disclose any plasma etching of the insulation layer for roughening the surface, roughening the surface before carrying out a plating for getting strong and reliable adhesion is known in the art and there are various methods known for the said roughening of the surface and the degree of roughening will depend upon the specific requirement. Enomoto discloses, though not plasma etching, one such method of roughening a resin surface

Art Unit: 2827

the art.

layer for better adhesion of conductor on the insulating layer. Further, Burke disclose plasma etching a polymeric film surface to roughen or create the micro profile for getting high peel strength between the metal and the film and Yasumoto, though not on insulating layer but on metallized layer, discloses plasma-etched irregularities having a difference of elevation of about 0.5 to about 200 nm. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Shinada with a surface roughness as claimed in order to have strong and reliable adhesion strength. Furthermore, it has been held that discovering an optimum value of a result effective variable involve only routine skill in

Page 6

Regarding claim 21, Shinada further discloses insulating layer comprises an epoxy resin and a polyamide resin.

Regarding claim 22, though Shinada does not disclose the plasma etching rate of the individual component of the composite insulating resin layer, Shinada disclose a resin composition of polyamide resin and epoxy resin, and as disclosed by the applicant the polyamide resin have relatively higher dry etching rate than epoxy resin.

Regarding claim 23, Shinada further discloses insulation layer comprise polyamide resin and epoxy resin.

Art Unit: 2827

trol Number: 09/539,864 Page 7

Regarding claim 26, though Shinada does not disclose reactive ion plasma etching with argon gas, such plasma etching process is known in the art and a suitable process can be used depending upon the specific requirement. Further, Burke disclose the reactive plasma etching process with argon gas for plasma etching a polymeric film, see Burke column 4, line 65-67 and column 5, line 1-4. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Shinada with insulating layer etched using reactive ion plasma etching with argon gas in order to have better peel strength and resistance to thermal cycle.

Response to Arguments

8. Applicant's arguments filed 9/9/02 have been fully considered but they are not persuasive.

Applicant's argument (about the prior art of Shinada, Burke and Yasumoto):

Shinada not using plasma etching of insulating layer,

Burke using plasma etching but not on resin composition as claimed by the applicant,

Yasumoto uses plasma etching the metallized surface and not the insulating layer.

Examiner's answer:

Claim 19 is a structural claim. Shinada does not disclose the method used by the applicant to manufacture the circuit board structure, but the structure as disclosed by

Art Unit: 2827

the prior art of Shinada is same as the structure claimed by the applicant. The structure can be made by various known methods depending upon the specific requirement, however the process limitation in a product claim defines the claimed invention over the prior art to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over the prior art. See Product-by-Process in MPEP 2113 and

Burke, Yasumoto and Enomoto, new prior art, are used as secondary reference to the extent that they disclose the use of roughening the surface for better and reliable adhesion property to be imparted to the final circuit board structure, including the reactive ion plasma etching with argon gas.

2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Boyko et al., disclose roughened dielectric layer made by using roughened metal layer.

Nakamura discloses sandblasting method for roughening the insulating layer.

Kinoshita and Yasue et al., discloses roughening resin composition surface by using oxidizing agent.

Gan discloses a resin composition for making metallic laminate.

Page 8

Art Unit: 2827

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703)

305 2617. The examiner can normally be reached on M-F (6:30 - 4) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

ibp

September 30, 2002

ALBERT W. PALADINI
PRIMARY EXAMINED

Page 9